

FIG.1

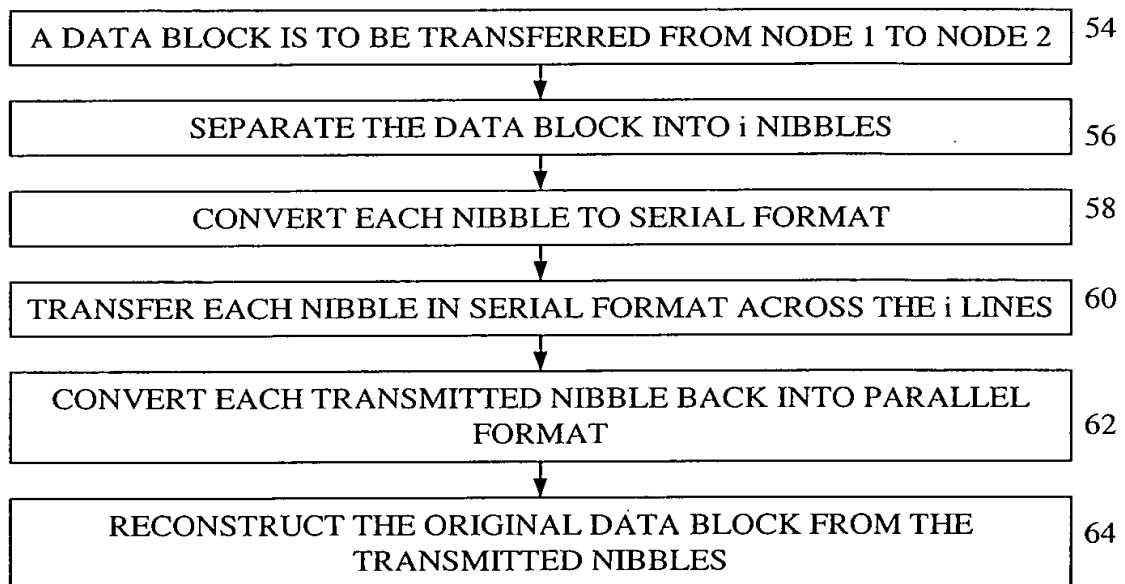


FIG.3

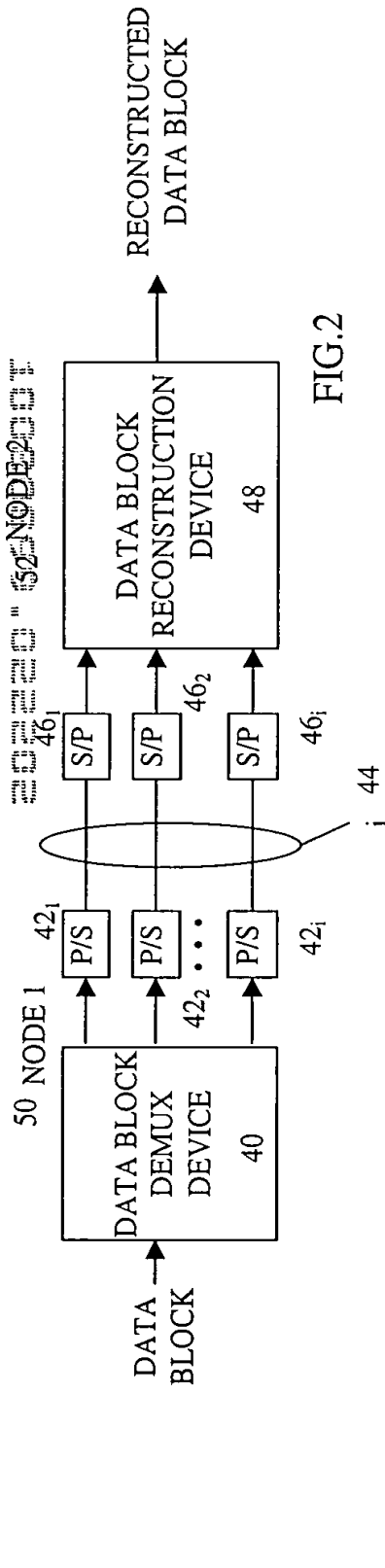


FIG. 2

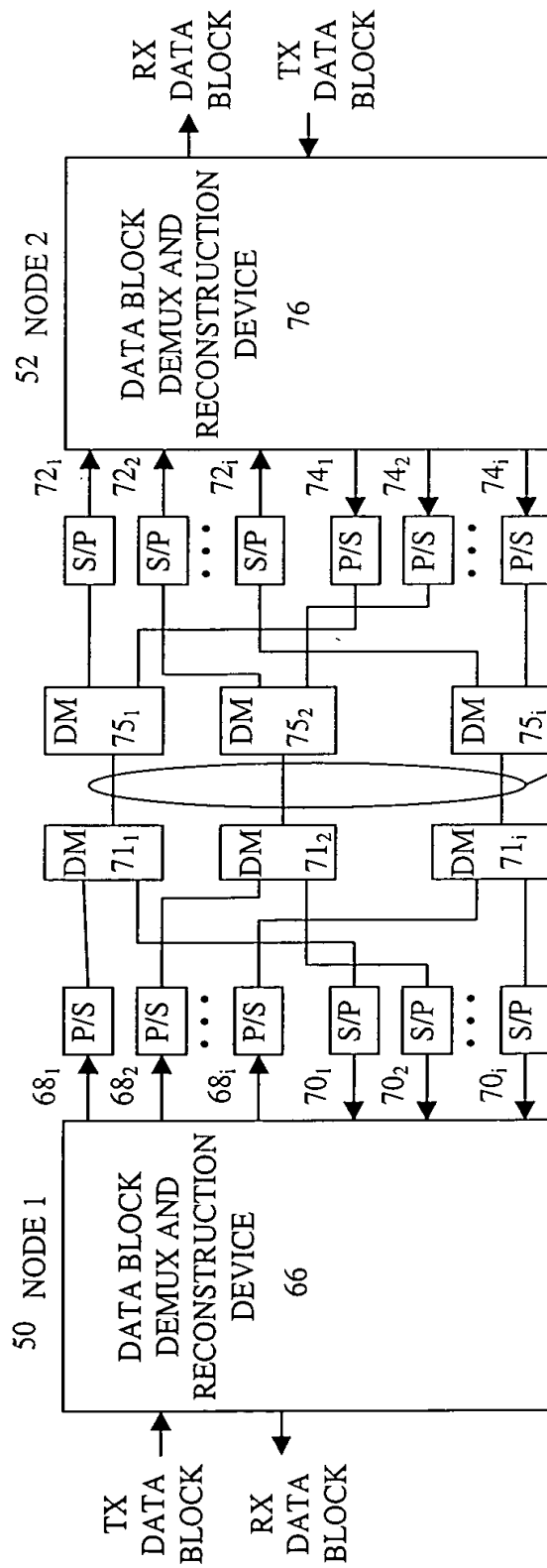


FIG. 6

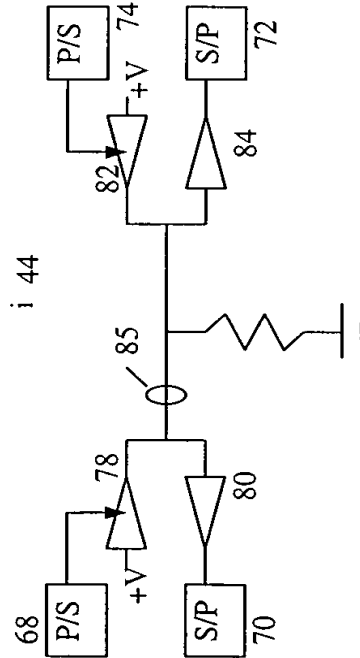


FIG. 7

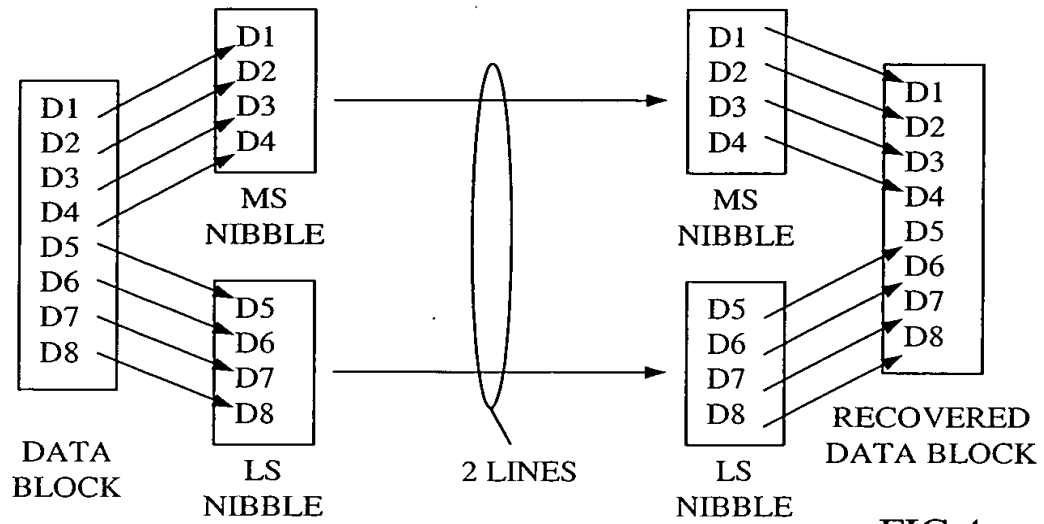


FIG.4

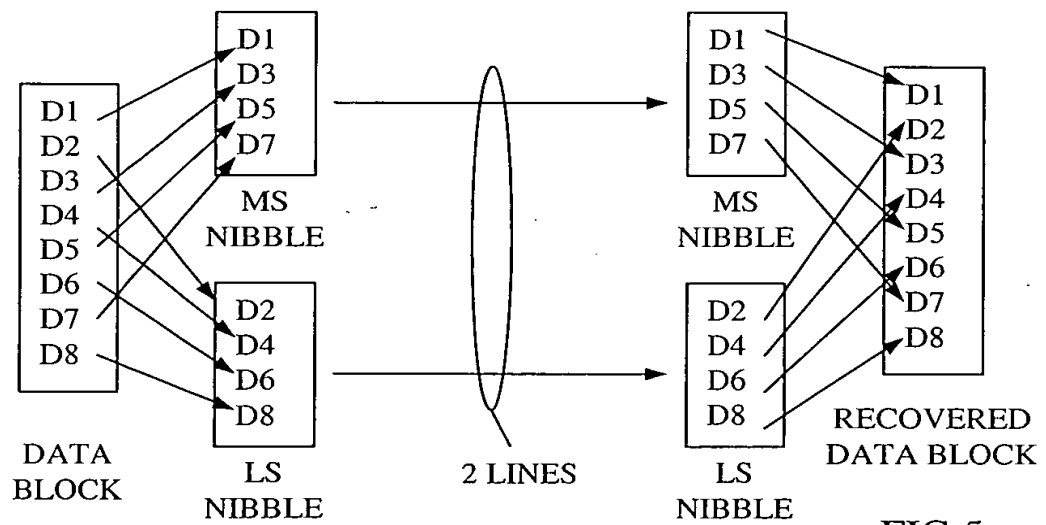


FIG.5

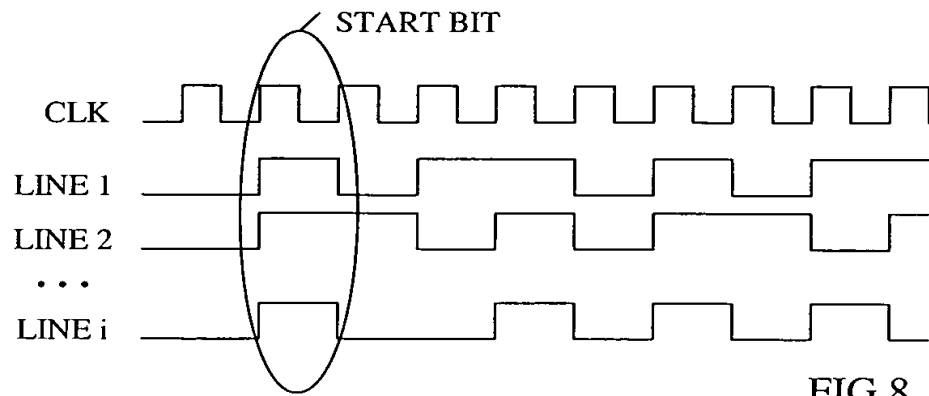


FIG.8

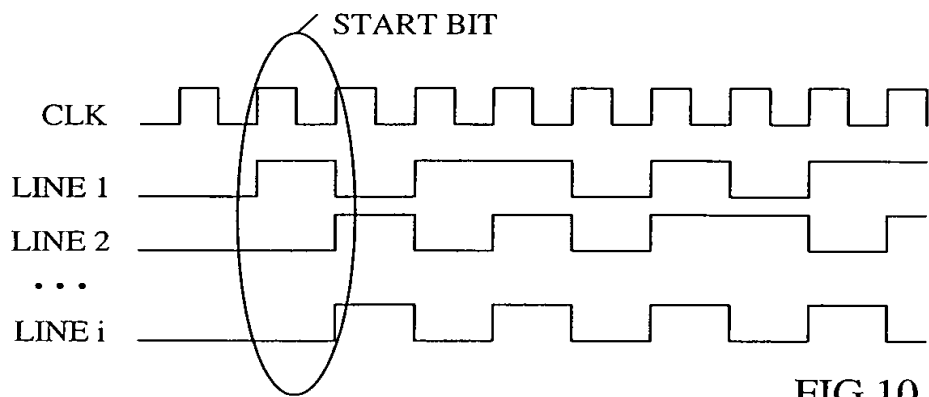


FIG.10

FUNCTION	LINE 1	LINE 2
ABSOLUTE VALUE	1	1
RELATIVE INCREASE	1	0
RELATIVE DECREASE	0	1
NO DATA TRANSFERRED	0	0

FIG.11

FUNCTION	LINE 1	LINE 2
DEVICE 1	1	1
DEVICE 2	1	0
INVALID	0	1
NO DATA TRANSFERRED	0	0

FIG.13

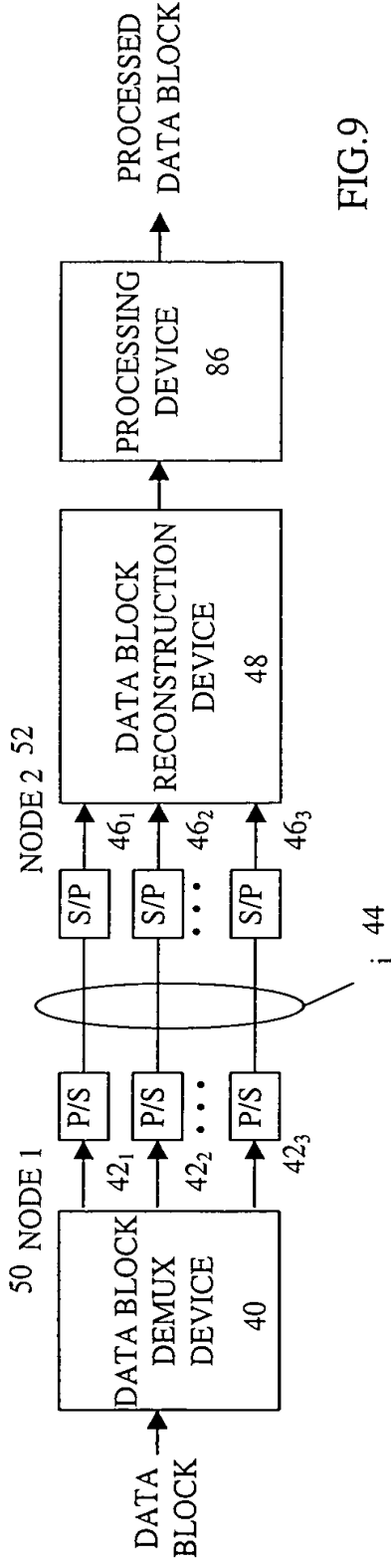


FIG. 9

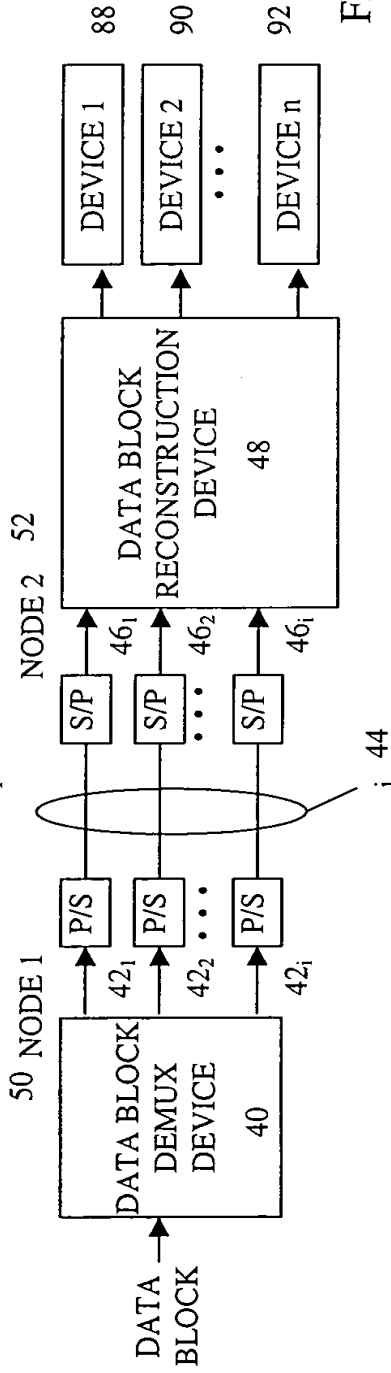


FIG. 12

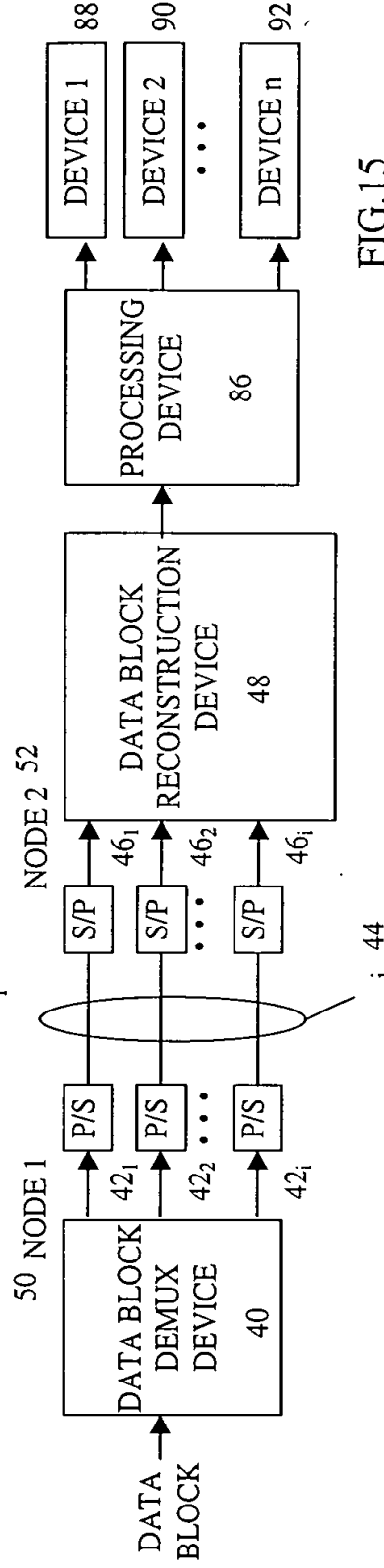


FIG. 15

FUNCTION/DEVICE	LINE 1	LINE 2	LINE 3
ABSOLUTE VALUE/DEVICE 2	1	1	1
ABSOLUTE VALUE/DEVICE 1	1	1	0
RELATIVE INCREASE/DEVICE 2	1	0	1
RELATIVE INCREASE/DEVICE 1	1	0	0
RELATIVE DECREASE/DEVICE 2	0	1	1
RELATIVE DECREASE/DEVICE 1	0	1	0
INVALID	0	0	1
NO DATA TRANSFERRED	0	0	0

FIG.14

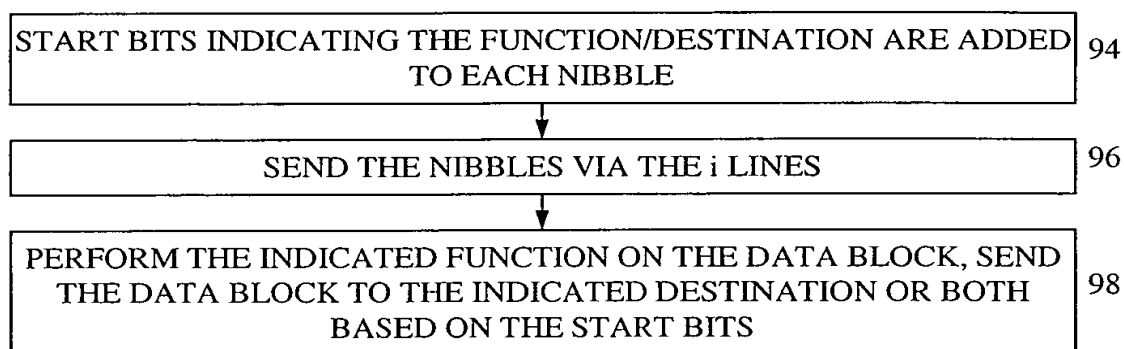


FIG.16

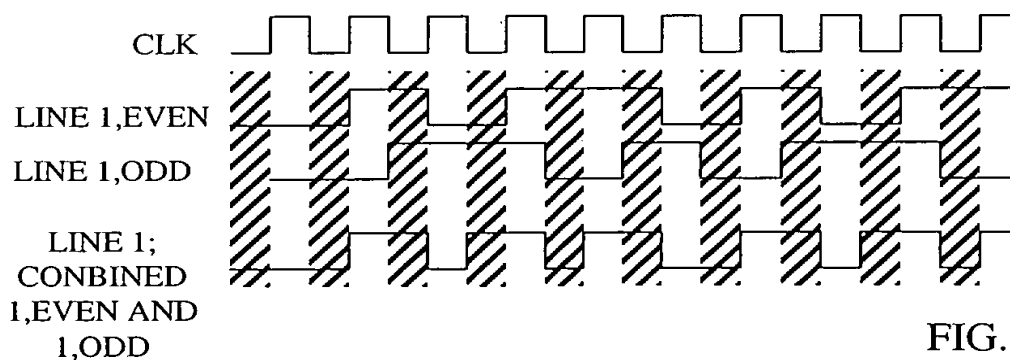


FIG.18

FIG. 17 is a block diagram of a data reconstruction system in accordance with the present invention.

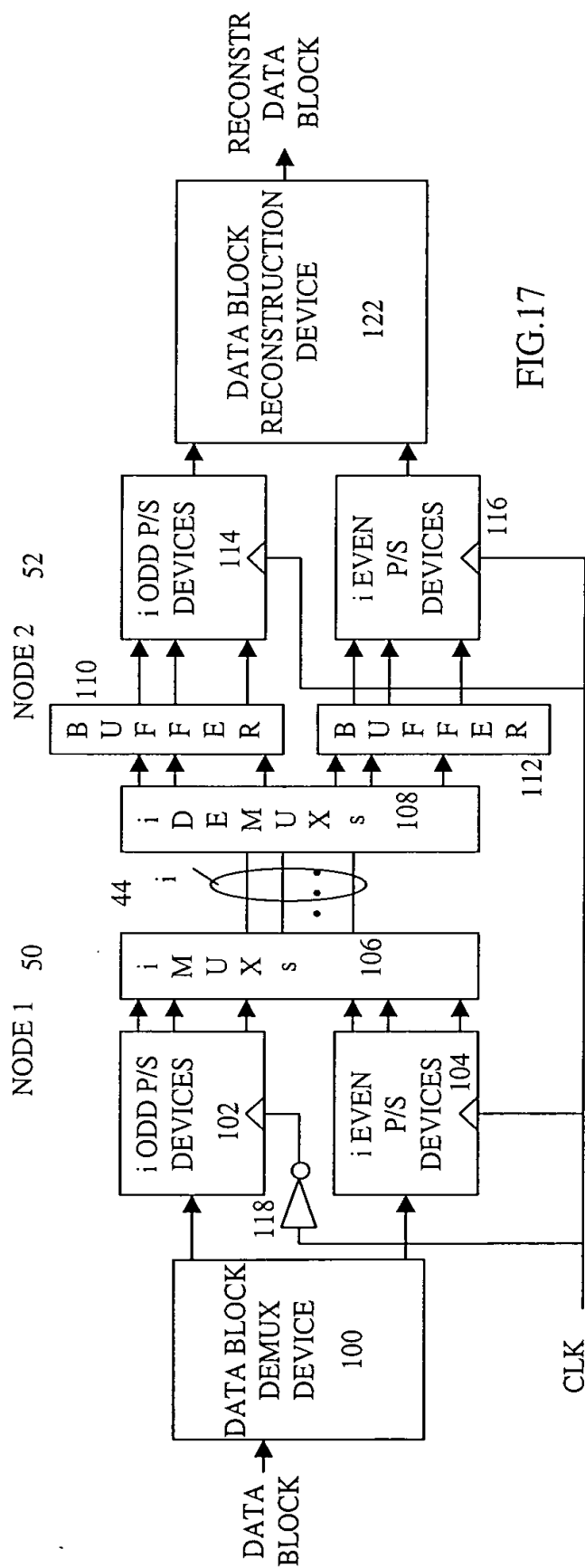


FIG.17

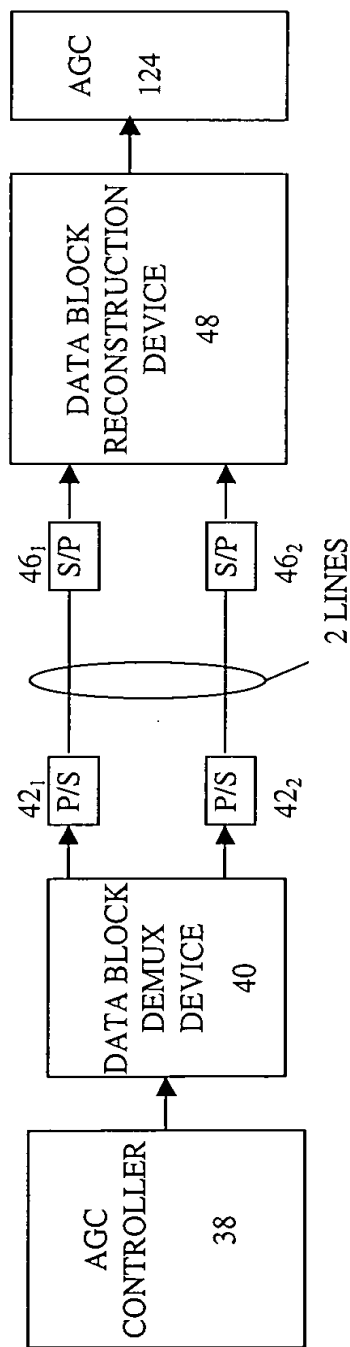


FIG.19

FIG. 20 is a block diagram of a system for processing data blocks. The system includes an AGC Controller 38, a Data Block Demux Device 40, a Data Block Reconstruction Device 48, an RX AGC 30, and a TX AGC 32. The AGC Controller 38 is connected to the Data Block Demux Device 40. The Data Block Demux Device 40 outputs three parallel data streams (42<sub>1</sub>, 42<sub>2</sub>, 42<sub>3</sub>) to three parallel P/S (Parallel-to-Serial) converters (46<sub>1</sub>, 46<sub>2</sub>, 46<sub>3</sub>). These converters are connected to three parallel S/P (Serial-to-Parallel) converters (46<sub>1</sub>, 46<sub>2</sub>, 46<sub>3</sub>). The S/P converters are connected to the Data Block Reconstruction Device 48. The Data Block Reconstruction Device 48 is connected to the RX AGC 30 and the TX AGC 32. The RX AGC 30 and TX AGC 32 are connected to each other. The system is labeled as 3 LINES 44.

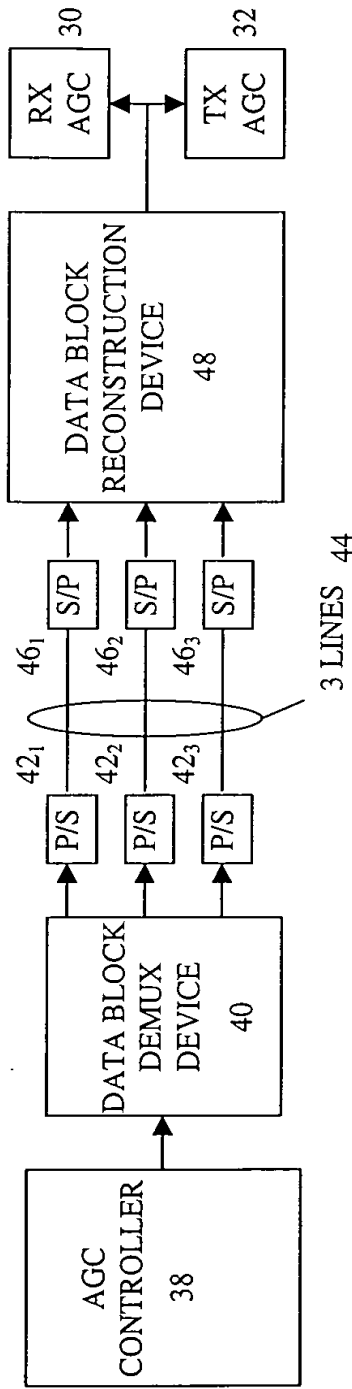


FIG. 20